REMARKS

In the Final Office Action of July 25, 2006, the Examiner (1) rejected claims 1-11 under U.S.C. § 102(e), as being anticipated by Patel (U.S. Pat. No. 6,826,749); (2) rejected claims 12-16, 18-24, and 26-27 under U.S. C. § 103(a) as being obvious over Patel in view of "Computer Architecture: A Qualitative Approach ("Hennessy"); (3) rejected claim 25 as obvious over Patel, Hennessy, Hendler (U.S. Pat. No. 6,473,777) and Brassac (U.S. Pat. No. 6,928,539); and (4) rejected claims 30-41 as obvious over Patel in view of Hendler. In this Response, Applicants amend claims 1-4, 6, 8, 10, 12, 13, 19, 27, 30, 35-37, and 41. Based on the amendments and arguments contained herein, Applicants respectfully request reconsideration and allowance.

By way of an introductory note and without further limiting the claims, Applicants' contribution includes the development of a processor core that can execute stack-based instructions (e.g., Java instructions). Various features are also implemented in Applicants' core to accelerate the execution of code. For example, a hardware-based stack is included in the core. This stack comprises replicated storage for the top *n* (e.g., 8) entries of a main stack implemented in memory outside the core. Although this core-based stack may become incoherent with regard to the main stack, typically only the top 8 or so entries are needed to process Java instructions. Accessing the core-based stack is faster than accessing a memory-based stack outside the core. Further, Applicants' core can execute, not only the stack-based instructions, but also instructions from another instruction set that contains memory-based and register-based instructions. By being able to also execute memory and register-based instructions, the execution of stack-based instructions can be made to run more efficiently and faster than if only stack-based instructions were permitted to be run on the core.

Turning now to the claims, claim 1 has been amended in several respects. Claim 1 has been amended to recite that the multi-entry stack, logic and the registers are all contained in the processor's core. This is in contrast to Patel which discloses the stack 50 and the registers 46, 48 are located outside the CPU core 26.

Further, claim 1 now requires the logic to execute "instructions from both said stack-based instruction set and said second instruction set" (the second instruction provides "register-based and memory-based operations"). The Java accelerator 42 converts Java instructions to native instructions and provides the converted instructions to the CPU 26. Col. 4, ll. 1-9. Thus, Patel's CPU core 26 does not execute stack-based instructions.

For any or all of these reasons, claim 1 and all of its dependent claims are allowable over Patel. No other art of record satisfies the deficiencies of Patel. Dependent claims 2-4 and 6 have been amended merely to maintain consistency with the amended language of claim 1.

Claim 8 has been amended to require that the fetch logic of the core retrieves instructions from the first and second instructions and that all of such instructions from both instructions are executed in the core. As explained above, Patel does not teach or even suggest these features. Patel's CPU core 26 does not fetch and execute stack-based instructions. For at least these reasons, claim 8 and all claims dependent thereon are in condition for allowance. Applicants amend claim 10 to maintain consistency with the amended language of claim 8.

Claim 12 has been amended in a similar fashion to claim 1. Thus, claim 12 and its dependent claims are in condition for allowance for much the same reason as claim 1. Dependent claims 13 and 19 have been amended merely to maintain consistency with the amended language of claim 12.

Claim 30 contains limitations that are not disclosed in the art of record as should be apparent from the preceding discussion. For example, the "hardware stack" recited in claim 30 is not disclosed in the art of record nor does the art of record disclose a core that is configured to execute stack-based instructions as well as memory-based and register-based instructions. For at least these reasons, claim 30 and its dependent claims are allowable. Claims 35-37 and 41 have been amended to maintain consistency with the amended language of claim 30.

Applicants hereby request a one-month time extension and authorize the Office to charge Texas Instruments Inc.'s Deposit Account No. 20-0668 for such fees. Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims), Examiner is authorized to charge Texas Instruments Inc.'s Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

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